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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
JOHNSTON, PHILLIP A	

ART UNIT	PAPER NUMBER
2881	

DATE MAILED: 11/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/817,270	INANAMI ET AL.4	
	Examln r	Art Unit	
	Phillip A Johnston	2881	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

Claims Rejection – 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-21, are rejected under 35 U.S.C. 103(a), as being unpatentable over U.S. Patent No. 5,371,373 to Shibata, in view of Shimada, U.S. Patent No. 5,348,902, and in further view of Murai, U.S. Patent No. 5,250,812.

Regarding Claims 1-4, and 6-21, Shibata (373) discloses in FIG. 3, an LSI device pattern supplied from the LSI CAD/DA system 1 to an electron beam (EB) lithography data conversion system 2 as input data to be converted into data having such a format as readable by an EB lithography apparatus. If the input data represents such a repeated pattern (which is also called a cell in some LSI-CAD systems) as, for example, patterns of a memory device, then a cell projection lithography technique is utilized to perform efficient writing or delineating operation (the standard cell library recording means, as recited in Claim 7). In this case, the input

data is processed by an EB lithography data generation system 3 of the cell projection lithography. The lithography data generated by the data conversion system 2 and the data generation system 3 (a lithography data generator and a pattern selector) is transferred to an EB lithography control system 4 and registered therein. Further, the repeated pattern processed by the EB lithography data generation system 3 of the cell projection lithography is generated as a second transfer mask 21 and installed in a second transfer mask mechanism 20 (the first placement positions of shaping holes on the CP aperture related to standard cells, as recited in Claim 1). See Column 4, line 24-44.

Shibata (373) also discloses an electron beam lithography method that includes steps of judging whether or not the number of the classified repetitive patterns is larger than or equal to a predetermined repetition number, and further classifying the classified repetitive patterns as non-repetitive patterns when it is judged that the number of the classified repetitive patterns is smaller than the predetermined repetition number (the aperture decision means for selecting a CP aperture having a throughput higher than a desired throughput, as recited in Claim 1). See Column 2, line 38-46.

Although the use of a standard cell library in the CAD system of Shibata (373) is implied, the terminology describing the standard cell library, as recited in Claims 1,4, and 6-21 is not specifically disclosed therein. Shimada (902); however, discloses that, in an automatic placing and routing system for fabricating a semiconductor integrated circuit device (hereinafter sometimes referred to simply as "LSI device"), cells are placed and routed between terminals on a semiconductor substrate. The cells include

basic cells of a standard cell system or a cell-based system, and are registered in a library as a functional block of, for example, a flip-flop or a two-input NAND gate. The layout of these cells is prepared through an automatic cell layout preparation program on the basis of a circuit diagram designed in advance. This automatic cell layout preparation program is for generating an actual cell pattern on the basis of circuit diagram information, a layout rule on the fabrication process of the LSI device and performance designating information such as the width and length (W/L) of the transistor. Design automation (DA) systems for automatic placing and routing of basic cells include those marketed by various computer-aided design (CAD) system makers and those internally fabricated by semiconductor integrated circuit device makers.

A cell with a pattern designed by the above-mentioned method is regarded as a basic cell of a standard cell system of a semiconductor integrated circuit and is registered in the library. A multiplicity of cells registered in the library are placed and routed in order to constitute a semiconductor integrated circuit device as required, and mask patterns are formed from information thus obtained (the decision means for conducting logic synthesis for CP apertures using standard cells, as recited in Claim 1). These masks are used for forming a semiconductor integrated circuit device on a semiconductor substrate. See Column 1, line 14-34; and Column 4, line 1-7.

Therefore, it would have been obvious to one of ordinary skill in the art, that the LSI/CAD data of Shibata's (373) lithography exposure system can be modified to use the standard cell library data of Shimada (902), making it possible to select the repetitive standard cells to be included on the mask .

Shibata (373) further discloses in Figure 1, the operations executed by the EB lithography data conversion system 2 and the cell projection lithography data generation system 3. In step 49 LSI pattern data is read and input from the LSI-CAD/DA system 1. In the next step 50, the input data is classified into repetitive patterns or non-repetitive patterns based on the cell name and array structure of the input pattern data and previously temporarily registered. When the input data is classified as the repetitive patterns in step 50, the processing proceeds to step 51, where it is determined whether or not a cell projection condition 1 is satisfied. The cell projection condition 1 is such that the repetitive numbers of the repetitive patterns is sufficiently large, as recited in Claims 1,7, and 15. In step 52, the repetitive unit pattern mask is thus set and the repetitive structure is simultaneously set, and then they are registered. Then, the processing proceeds to step 53, whereat the non-repetitive patterns temporally registered are extracted in step 50 and the extracted patterns are subjected to a normal lithography data conversion. In step 54, a preparing operation (mask layout and lithography data conversion) of the second transfer mask is carried out and the mask is set in the second transfer mask mechanism 20 in step 55.Then, the processing proceeds to step 56, where the mask and repetitive structure registered in step 52 are selected and composed with the lithography data of the non-repetitive pattern obtained in step 53. Next, the processing proceeds to step 57, where the lithography data obtained in step 56 is sorted according to the lithography sequence and output as lithography data. See Column 6, line 53-68, and Column 7, line 1-37.

Shibata (373) still further discloses that after the lithography data for delineating and the second transfer mask 21 are generated in this way, the EB lithography control system 4 transfers the lithography data through a system bus 7 to a buffer memory 5 at a high speed. The buffer memory 5 is usually formed of two memory units so that while one of the memory units is receiving the lithography data through the system bus 7, the other of the memory units is transferring the lithography data to a data control system 8 at a high speed for the body of the apparatus in its delineating operation. Further, in order to convert the shot patterns into a beam, the shot patterns are controlled and calibrated through a transfer/deflection system 10 and a lens system 11 in an analog control system 9 and then irradiated as a beam 17 onto an object 15 to be delineated. See Column 4, line 44-54.

It should be noted that the lithography control system 4 of Shibata (373) as described above uses two memory units, one utilizes the lithography data to control passage of the electron beam through the standard cell apertures in the mask and the other uses the lithography data to control the process of delineating placement of the selected standard cells on the substrate, by deflecting the electron beam to form the desired pattern.

Regarding Claim 5, Shibata (373) in view of Shimada (902) above does not disclose a mask containing cell projection apertures and an opening for a variable shaped beam (VSB). Murai (812); however, discloses in FIG. 10B, a partial plan view of the aperture plate 108 and shows a group of apertures for fixed shaped beams with

five kinds of apertures 102, 103, 104, 105 and 106 and an aperture 107 for obtaining a variable shaped beam. See Column 7, line 50-68; and Column 8, line 1-15.

Therefore, it would have been obvious to one of ordinary skill in the art, that the lithography exposure system of Shibata (373) in view of Shimada (902) can be modified to use the mask containing both cell projection apertures and an opening for VSB in accordance with Murai (812), to increase lithography throughput.

Conclusion

4. Any inquiry concerning this communication or earlier communications should be directed to Phillip Johnston whose telephone number is (703) 305-7022. The examiner can normally be reached on Monday-Friday from 7:30 am to 4:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor John Lee can be reached at (703) 308-4116. The fax phone numbers are (703) 308-2864 and (703) 308-7721.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 0956.

PJ
October 24, 2003

JOHN R. LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800